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10/804,737	03/18/2004	Ikuroh Ichitsubo	MicroMobio-005	8276

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EXAMINER	
LEWIS, MONICA	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/804,737	ICHITSUBO ET AL.	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the pre-appeal brief filed February 19, 2007.

Response to Arguments

2. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-9, 11, 14, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent No. 6,642,617) in view of *Active Substrates* by Steve Riches and Tomura et al. (U.S. Patent No. 5,628,919).

In regards to claim 1, Kawai discloses the following:

a) one or more active substrates (12a) comprising substantially transistors or diodes (10) formed thereon (For Example: See Figure 3 and Column 5 Lines 45 and 46);

b) one or more passive substrates (2a) comprising substantially inductors, capacitors or resistors (4) formed thereon (For Example: See Figure 3 and Column 4 Lines 17-20);

c) a plurality of bonding pads (15a and 5b) positioned on the active and passive substrates (For Example: See Figure 1); and

d) bonding wires (6) connected to the bonding pads (For Example: See Figure 1).

In regards to claim 1, Kawai fails to disclose the following:

a) a plurality of active substrates.

However, Riches discloses a semiconductor device that has a plurality of active substrates (For Example: See Page 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include a plurality of active substrates as disclosed in Riches because it aids in providing a support for the interconnection of various components (For Example: See Page 1).

Additionally, since Kawai and Riches are both from the same field of endeavor, the purpose disclosed by Smiths would have been recognized in the pertinent art of Riches.

b) intra-substrate pads adapted to support wire-bonding within a substrate.

However, Tomura et al. ("Tomura") discloses a semiconductor device that has intra-substrate pads adapted to support wire-bonding within a substrate (For Example: See Figure 1). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include intra-substrate pads adapted to support wire-bonding within a substrate as disclosed in Tomura because it aids in providing interconnection (For Example: See Figure 1 and Abstract).

Additionally, since Kawai and Tomura are both from the same field of endeavor, the purpose disclosed by Tomura would have been recognized in the pertinent art of Kawai.

In regards to claim 2, Kawai discloses the following:

a) a die pad (12b and 2b)to receive the active and passive substrates (For Example: See Figure 1).

In regards to claim 3, Kawai discloses the following:

a) the substrates comprise gallium arsenide substrates (For Example: See Column 3 Lines 19-22 and Column 4 Line 42).

In regards to claim 4, Kawai discloses the following:

a) the active and passive substrates comprise gallium arsenide (For Example: See Column 3 Lines 19-22 and Column 4 Line 42).

In regards to claim 5, Kawai discloses the following:

a) the active substrate comprises supporting passive components (For Example: See Column 4 Lines 34-51).

In regards to claim 6, Kawai discloses the following:

a) a passive IC coupled to the active substrate (For Example: See Figure 1).

In regards to claim 7, Kawai discloses the following:

a) one or more substantially passive ICs for passive components only (For Example: See Figure 1).

In regards to claim 8, Kawai discloses the following:

a) the active and passive substrates are interconnected with bonding wires (For Example: See Figure 1).

In regards to claim 9, Kawai discloses the following:

a) the active and passive substrates are mounted on a metal die pad (For Example: See Figure 1).

In regards to claim 11, Kawai discloses the following:

a) the active substrates comprise primarily transistors (For Example: See Column 5 Lines 45 and 46).

In regards to claim 14, Kawai discloses the following:

a) the passive substrate comprises a network of resistor, inductor, and capacitor (For Example: See Column 4 Lines 17-20).

In regards to claim 19, Kawai discloses the following:

a) the passive substrate comprises one or more circuits of passive components including transmission lines, impedance matching network, filters, baluns, or diplexers (For Example: See Column 3 Lines 4-18).

In regards to claim 20, Kawai fails to disclose the following:

a) the passive substrate is fabricated using fewer fabrication steps than the active substrate.

Finally, the following limitation makes it a product by process claim: a) "fabricated using fewer fabrication steps." The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent No. 6,642,617) in view of *Active Substrates* by Steve Riches, Tomura et al. (U.S. Patent No. 5,628,919) and Lin (U.S. Publication No. 6,806,578).

In regards to claim 3, Kawai fails to disclose the following:

a) one or more pins and wherein one or more bonding wires connect one or more bonding pads to the one or more pins.

However, Lin discloses a semiconductor device that has a one or more pins and wherein one or more bonding wires connect one or more bonding pads to the one or more pins (For Example: See Paragraph 29). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include one or more pins wherein one or more bonding wires connect one or more bonding pads to the one or more pins as disclosed in Lin because it aids in increasing the ESD protective capability (For Example: See Paragraph 15).

Additionally, since Kawai and Lin are both from the same field of endeavor, the purpose disclosed by Lin would have been recognized in the pertinent art of Kawai.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent No. 6,642,617) in view of *Active Substrates* by Steve Riches, Tomura et al. (U.S. Patent No. 5,628,919) and *Electronic Packaging and Interconnection Handbook* by Charles A. Harper.

In regards to claim 10, Kawai fails to disclose the following:

a) the substrates are encapsulated in molded plastics or other insulating medium.

However, Harper discloses a semiconductor device that has substrates encapsulated in molded plastic (For Example: See Page 7.20). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of

Kawai to include substrates encapsulated in plastic as disclosed in Harper because it aids in providing better performance at a low cost (For Example: See Page 7.20).

Additionally, since Kawai and Harper are both from the same field of endeavor, the purpose disclosed by Harper would have been recognized in the pertinent art of Kawai.

6. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent No. 6,642,617) in view of *Active Substrates* by Steve Riches, Tomura et al. (U.S. Patent No. 5,628,919) and *Microchip Fabrication* by Peter Van Zant.

In regards to claim 12, Kawai fails to disclose the following:

a) the transistors include silicon, bipolar, CMOS, RFCMOS, BICOMS, SiGe, GaAs, HBT or HEMT.

However, Van Zant discloses a bipolar transistor (For Example: See Pages 507-508). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include a bipolar transistor as disclosed in Van Zant because it aids in providing fast switching speeds (For Example: See Page 509).

Additionally, since Kawai and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Kawai.

In regards to claim 13, Kawai fails to disclose the following:

a) the transistors are fabricated on a wafer with semiconductor layer structure, junctions and dopings.

However, Van Zant discloses a transistor with semiconductor layer structure, junctions and dopings (For Example: See Pages 507-508). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of

Kawai to include a transistor with a semiconductor layer structure, junctions and dopings as disclosed in Van Zant because that is well known that those components aid in forming a transistor (For Example: See Page 507-509).

Additionally, since Kawai and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Kawai.

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent No. 6,642,617) in view of *Active Substrates* by Steve Riches, Tomura et al. (U.S. Patent No. 5,628,919) and Pohjonen (U.S. Patent No. 6,462,950).

In regards to claim 15, Kawai fails to disclose the following:

a) the passive substrate comprises one or more conductive metal layers for inductor and interconnection.

However, Pohjonen discloses a semiconductor device that has a passive substrate that comprises one or more conductive metal layers for inductor and interconnection (For Example: See Column 5 Lines 20-26). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include a passive substrate that comprises one or more conductive metal layers for inductor and interconnection as disclosed in Pohjonen because it aids in stabilizing voltage power supply feeds (For Example: See Column 5 Lines 20-26).

Additionally, since Kawai and Pohjonen are both from the same field of endeavor, the purpose disclosed by Pohjonen would have been recognized in the pertinent art of Kawai.

In regards to claim 16, Kawai fails to disclose the following:

a) the passive substrate comprises an insulating layer with suitable dielectric properties.

However, Pohjonen discloses a semiconductor device that has a passive substrate that comprises an insulating layer with suitable dielectric properties (For Example: See Column 5 Lines 11-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include a dielectric layer as disclosed in Pohjonen because it aids in protecting the device (For Example: See Column 5 Lines 11-16).

Additionally, since Kawai and Pohjonen are both from the same field of endeavor, the purpose disclosed by Pohjonen would have been recognized in the pertinent art of Kawai.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent No. 6,642,617) in view of *Active Substrates* by Steve Riches, Tomura et al. (U.S. Patent No. 5,628,919) Pohjonen (U.S. Patent No. 6,462,950) and *Microchip Fabrication* by Peter Van Zant.

In regards to claim 17, Kawai fails to disclose the following:

a) the insulating layer comprises nitride or oxide as the dielectric layer for a capacitor.

However, Van Zant discloses silicon nitride (For Example: See Page 391). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include silicon nitride as disclosed in Van Zant because it aids in providing higher dielectric strength (For Example: See Page 391).

Additionally, since Kawai and Van Zant are both from the same field of endeavor, the purpose disclosed by Van Zant would have been recognized in the pertinent art of Kawai.

9. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai (U.S. Patent No. 6,642,617) in view of *Active Substrates* by Steve Riches, Tomura et al. (U.S. Patent No. 5,628,919) and Apel (U.S. Patent No. 6,727,761).

In regards to claim 18, Kawai fails to disclose the following:

a) the passive substrate comprises a layer including TaN or NiCr for a resistor.

However, Apel discloses a layer including TaN or NiCr for a resistor (For Example: See Column 3 Lines 13-16). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor of Kawai to include TaN or NiCr for a resistor as disclosed in Apel because it aids in controlling thermal runaway (For Example: See Abstract).

Additionally, since Kawai and Apel are both from the same field of endeavor, the purpose disclosed by Apel would have been recognized in the pertinent art of Kawai.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 571-272-1838. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization

where this application or proceeding is assigned is 571-273-8300 for regular and after final communications.

ML

May 17, 2007

MONICA LEWIS
PRIMARY PATENT EXAMINER